Application Note

Using the BLF1820-90 LDMOS Transistor for PCS band GSM and EDGE GSM Applications

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Philips Semiconductors

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Abstract

The following application note demonstrates the design and performance of an application circuit for the BLF1820-90 for PCS band EDGE GSM applications.

Revision history

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Keywords

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Summary

An application circuit is demonstrated to optimize the Philips BLF1820-90 LDMOS device for EDGE GSM performance in the 1930-1990 (PCS) transmit band. 45.5 dBm of output power is achieved with this device with significant margin to the overall EDGE GSM specs. The circuit was optized with efficiency as a goal as well. The device can be used in the circuit shown in adverse environmental conditions and still operate under suitable junction temperatures. This device is an appropriate choice for EDGE GSM systems in the DCS and PCS bands when 30W of nominal EDGE GSM operating power is required.

Contents

1. Introduction

As basestation providers begin to roll-out their next generation systems, devices must be able to perform well under a variety of modulation schemes. When EDGE GSM is employed to increase data rates, care must be taken such that the amplifier obtains excellent GSM performance as well. This application note shows the design and performance of the Philips BLF1820-90 LDMOS transistor operating in both GSM (CW) and EDGE GSM modes. The circuit has been designed to meet very stringent linearity specifications. These can be traded off to obtain a different compromise in performance. It will be shown what areas of the circuit must be modified to obtain these trade-offs.

The BLF1820-90 LDMOS transistor utilizes Philips Semiconductors' second generation LDMOS technology with gold top metallization. The device contains integrated input and output matching, which enables an amplifier design with high gain and good gain flatness over the band of interest. The device is available in both a standard as well as an earless package. The application note shows results in a circuit utilizing the standard package.

2. RF performance characteristics

Table 1 shows typical performance of the BLF1820-90 in a circuit optimized for EDGE GSM performance for 45.5 dBm output power. The tune was chosen to be an overall compromise of all the RF parameters, Gain, EVM, ORFS, and Efficiency. There will be a section later that shows how to trade off one parameter for another.

Parameter	Value
Frequency (MHz)	1930-1990
Test signal	EDGE GSM (all slots 'ON')
Supply voltage (V)	28.2
Idq (mA)	750
Power Gain (dB)	11.5 dBm (1960 MHz, 750 mA, 45.5 dBm Pout)
Gain flatness (dB)	0.45 dB (750mA, 45.5 dBm)
P1 dB (dBm)	> 48.4 dBm (test range limit)
Efficiency (%)	41% (48.4 dBm CW, 750 mA) 32% (45.5 dBm EDGE, 750 mA)
AVG RMS EVM (%)	1.5% (45.5 dBm, 750 mA, 1960 MHz)
400 KHz ORFS (dBc)	-61.5 dBc (45.5 dBm, 750 mA, 1960 MHz)
600 KHz ORFS (dBc)	-74 dBc (45.5 dBm, 750 mA, 1960 MHz)

3. Design of the amplifier

3.1 Mounting considerations

For good thermal contact, heatsink compound should be used when mounting the transistor to a heatsink. This is the method that was incorporated in this application note. For better thermal contact it is recommended to use the earless package and solder the transistor to a heatsink. When the device is soldered in, any parameters related to the device heating up will behave better. It would therefore be expected to achieve slightly better Error Vector Magnitude (EVM) and Output RF Spectrum (ORFS) when soldering the device in.

3.2 Bias circuit

The gate-source bias voltage is supplied through a voltage divider set by adjusting the potentiometer, R4 to control the optimum Idq (See the schematic in Figure 1). Idq was set to 750 mA to achieve the compromise demonstrated in this report. Section 6, 'Amplifier performance', will show the effect on the GSM gain performance when the bias current is changed. Deviations from this optimal bias point will result in suboptimal trade-offs of performance parameters such as gain compression and efficiency. The device is more linear, but less efficient for the tune shown here at higher drain voltages. If the user has severe efficiency requirements, 26V may be more suitable on the drain. If the user has more requirements for linearity, 30V on the drain may be more appropriate.

3.3 Circuit design

Both gate and drain supply are supplied by means of $\lambda/4$ lines. External matching networks are used to match the transistor impedances to 50Ω. The placement of the shunted ATC100B ceramic capacitors at the end of the $\lambda/4$ stubs is critical. Those capacitors should be placed such to minimize the self-resonance effects caused by these capacitors, i.e.: with the capacitor marking on the side. Additionally, the position of these shunt capacitors along the quarter wave line strongly influences performance. Improper placement of the ATC100B capacitors will reduce the amplifier gain.

4. Amplifier alignment

Figure 2 shows the layout of the circuit. Trade-offs in gain, efficiency, and linearity can be made by changing the extent of the tune of trimmers C5 and C8. Additionally, changes can be made with adjustments in the microstrip matching sections. The length and width of L7 and L9 are especially important in this regard.

In general, the following tuning guidelines should be considered in optimizing the circuit.

Effect of tuning trimmer on output:

Tuning ‘IN’ makes the efficiency and gain increase, at the expense of ORFS. The same effect will occur if the trimmer on the output is moved closer to the device.

Effect of tuning trimmer on input:

Tuning ‘IN’ increases gain, at the expense of EVM. This same effect will occur if the trimmer is moved closer to the device. Since EVM is the prime parameter of optimization for the tune shown in this application note, this is the first modified tune that may be tried.

First microstrip section off drain:

Adding width will lower the efficiency, and lower the gain. Reducing the width will make the ORFS worse.

5. Circuit diagram and pc-board layout

5.1 Circuit diagram

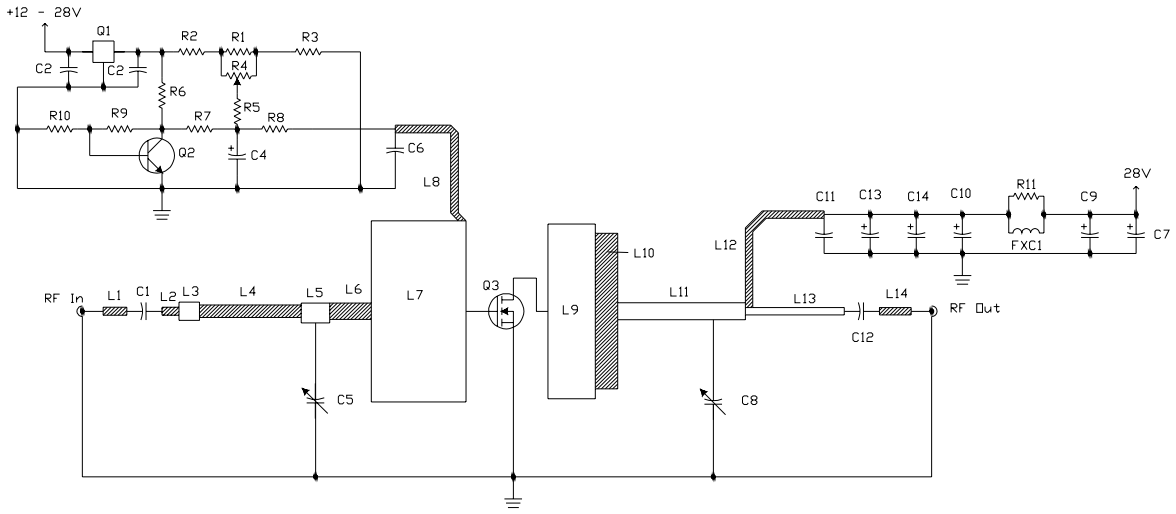


Figure 1. BLF1820-90 PCS band EDGE GSM Schematic

5.2 PC-board layout

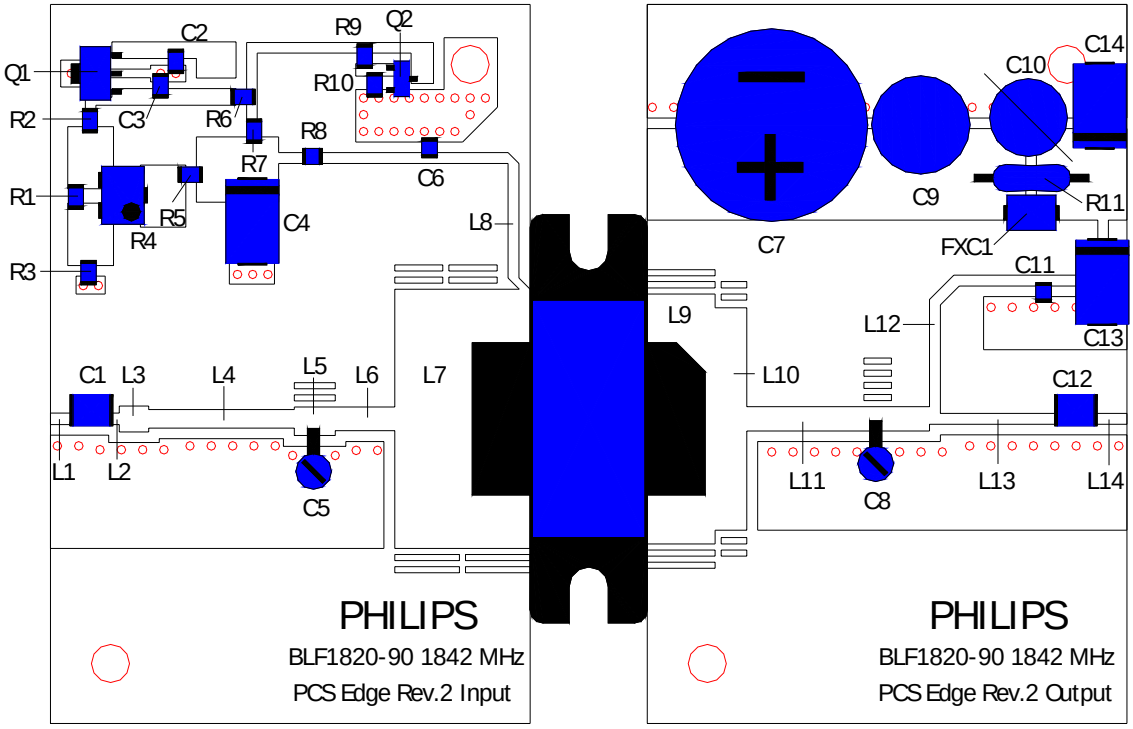


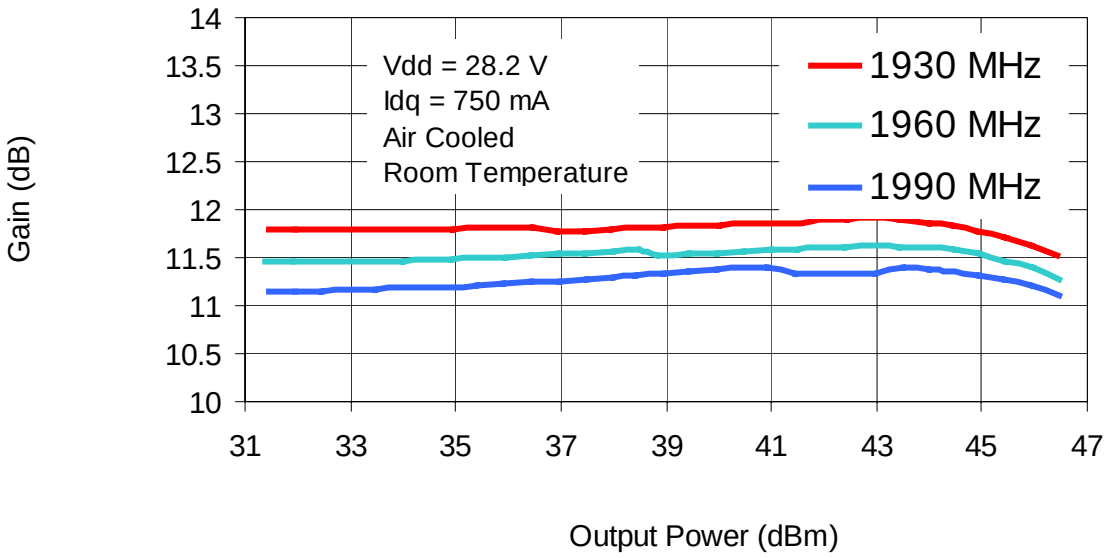
Figure 2. BLF1820-90 PCS band EDGE GSM layout

5.3 Component List

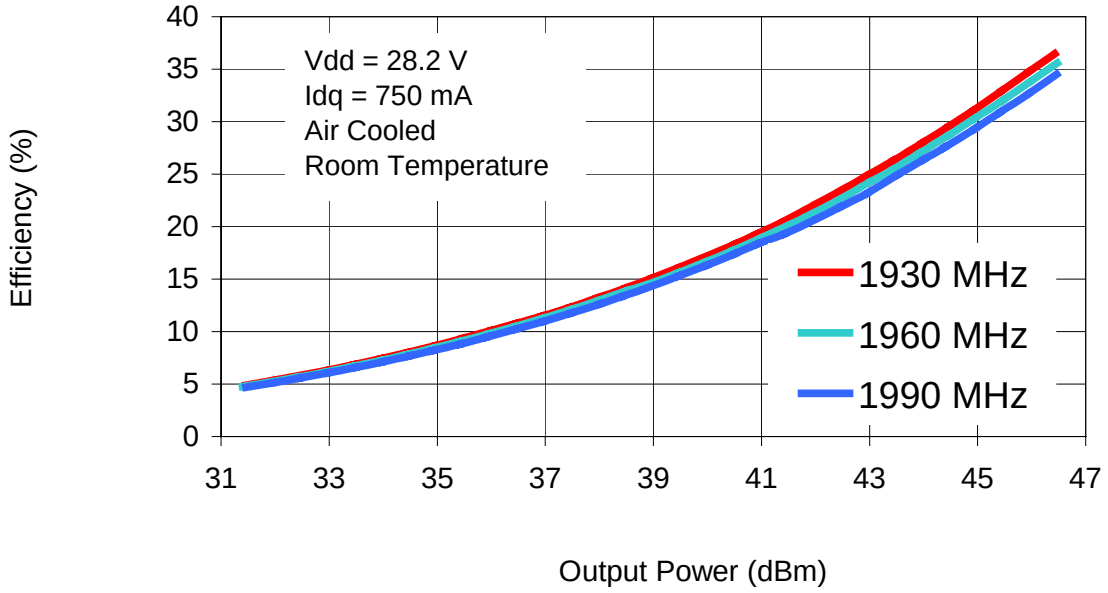
Component	Description	Value	length x width [mils]	Part Number
C1, C12	ATC Ceramic Capacitor	11pF		100B110KP
C2, C3	Newark Ceramic Capacitor	100nF		50N731
C4, C13	Newark Tantalum Capacitor	10uF		19C6240
C5, C8	Tronser Variable Capacitor	2pF		66-0304-00002-000
C6, C11	ATC Ceramic Capacitor	68pF		100A680KW
C7	Newark Electrolytic Capacitor	2200uF		44F2322
C9	Kigi-Key Electrolytic Capacitor	100uF		P5182-ND
C10	Newark Electrolytic Capacitor	47uF		95F4566
C14	Newark Tantalum Capacitor	10uF		19C6240
R1, R2	Resistor	430 Ohms		
R3	Resistor	750 Ohms		
R4	Potentiometer	200 Ohms		
R5	Resistor	3 Kohms		
R6	Resistor	1.1 Kohms		
R7	Resistor	11 Kohms		
R8	Resistor	9.1 Ohms		
R9	Resistor	6.2 Kohms		
R10	Resistor	910 Ohms		
R11	Resistor	10 Ohms		
FXC1	Newark FXC Bead			95F786
Q1	Voltage Regulator	8V		NJM78L08UA-ND
Q2	NPN Transistor			2N2222
Q3	Phlips LDMOS Transistor			BLF1820-90
L1	Microstrip		111 x 38	
L2	Microstrip		80 x 38	
L3	Microstrip		96 x 85	
L4	Microstrip		478 x 60	
L5	Microstrip		135 x 94	
L6	Microstrip		195 x 78	
L7	Microstrip		445 x 850	
L8	Microstrip		724 x 36	
L9	Microstrip		222 x 820	
L10	Microstrip		105 x 730	
L11	Microstrip		600 x 80	
L12	Microstrip		747 x 35	
L13	Microstrip		464 x 35	
L14	Microstrip		149 x 35	
PC Material	Rogers 6006, Er = 6.15		25 mil thick on 1 oz.	

6. RF Performance

BLF1820-90 EDGE Gain vs Power as a function of Frequency

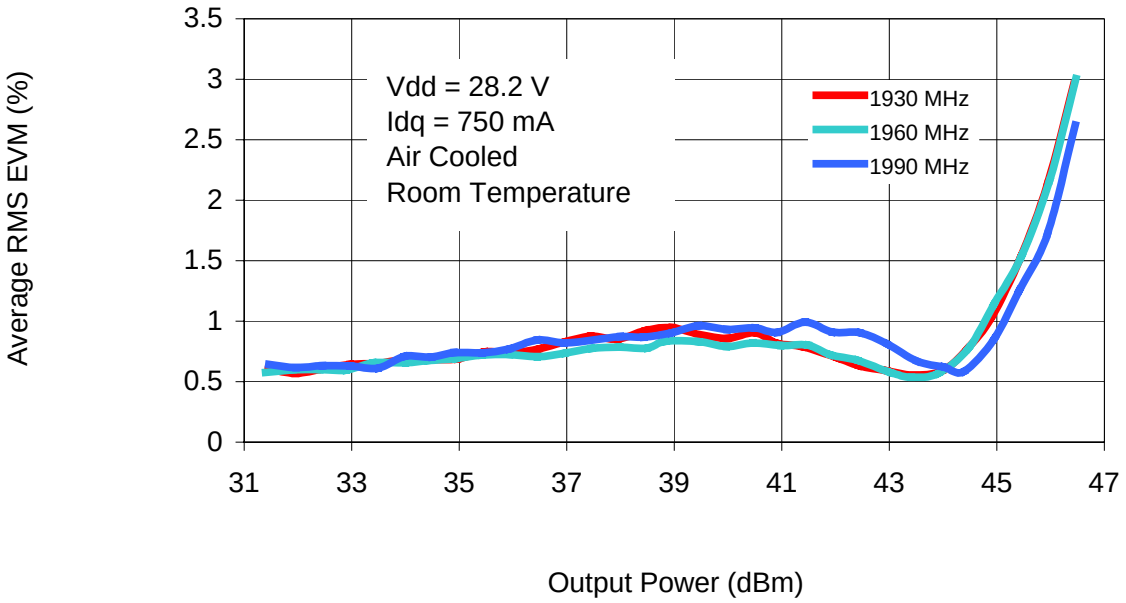


BLF1820-90 EDGE Efficiency vs Power as a function of Frequency

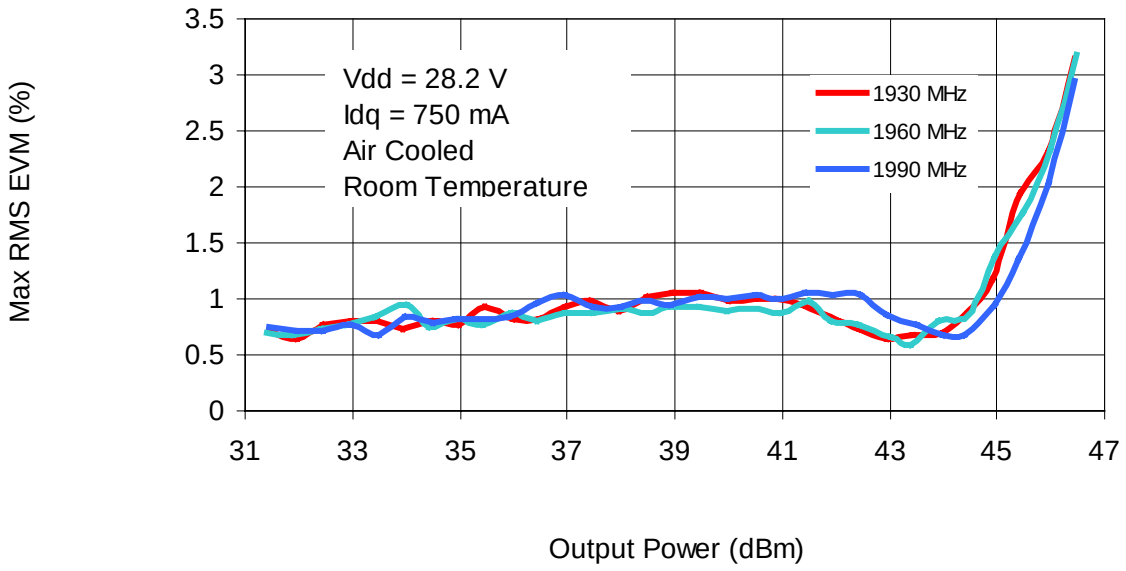


6. RF Performance (Continued)

BLF1820-90 AVG RMS EVM vs Power as a function of Frequency

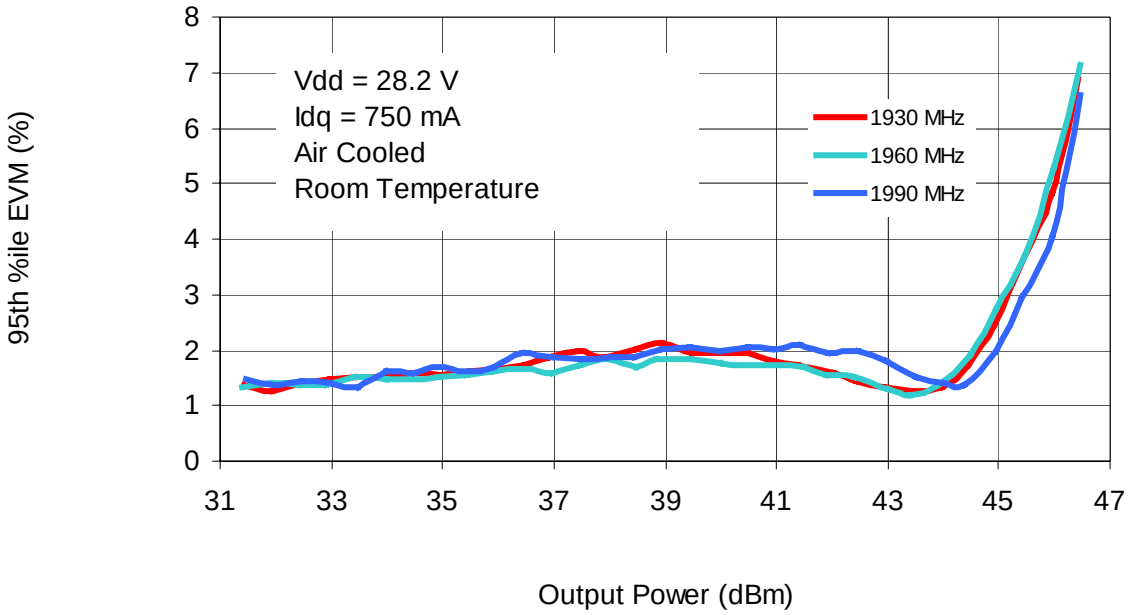


BLF1820-90 Max EVM vs Power as a function of Frequency

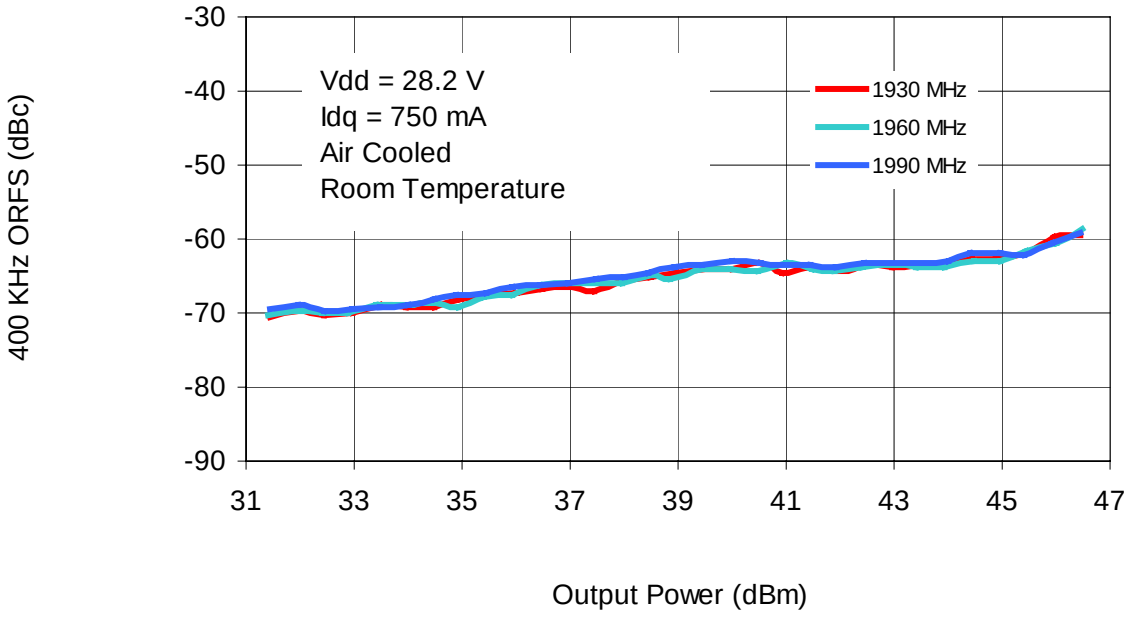


6. RF Performance (Continued)

BLF1820-90 95th %ile EVM vs Power as a function of Frequency

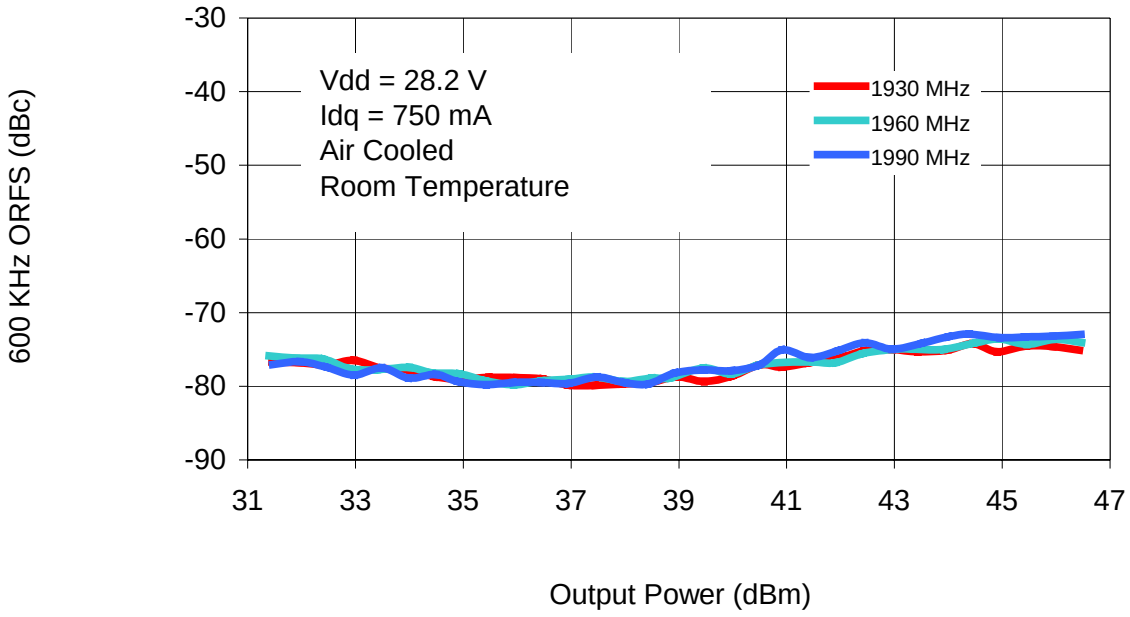


BLF1820-90 400 KHz ORFS vs Power as a function of Frequency

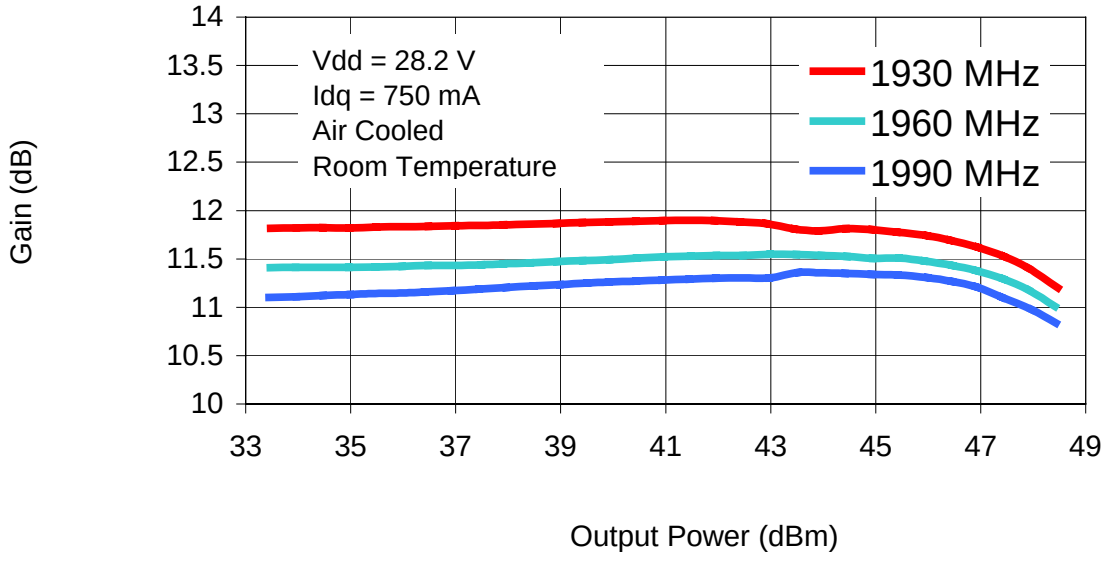


6. RF Performance (Continued)

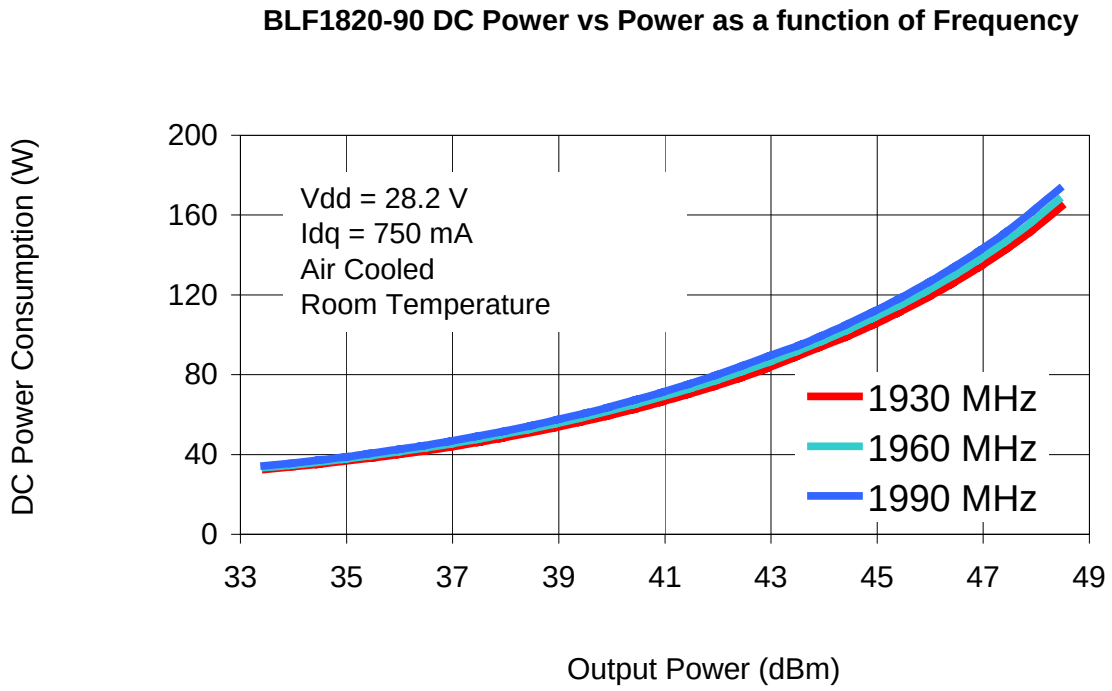
BLF1820-90 600 KHz ORFS vs Power as a function of Frequency



BLF1820-90 CW Gain vs Power as a function of Frequency



6. RF Performance (Continued)



7. Base plate drawing

The base plate consists of three parts. A brass input section to which the input pc-board is soldered, a brass output section to which the output pc-board is soldered, and a copper middle section on which the transistor is mounted. When the fixture is taken apart, the base plate provides mounting holes for SMA launchers in order to determine Zload and Zsource.

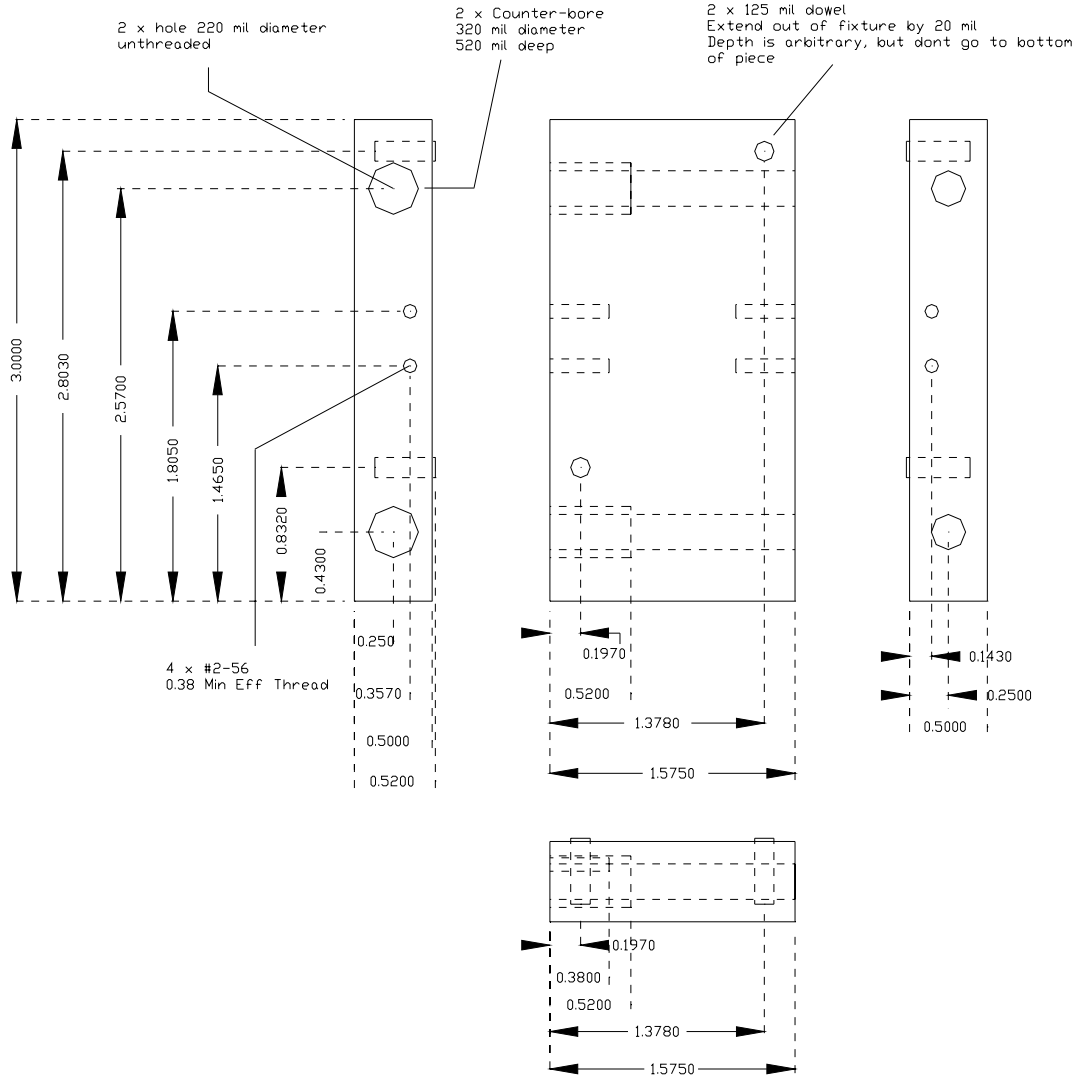


Figure 3. Brass Input Fixture

7. Base plate drawing (Continued)

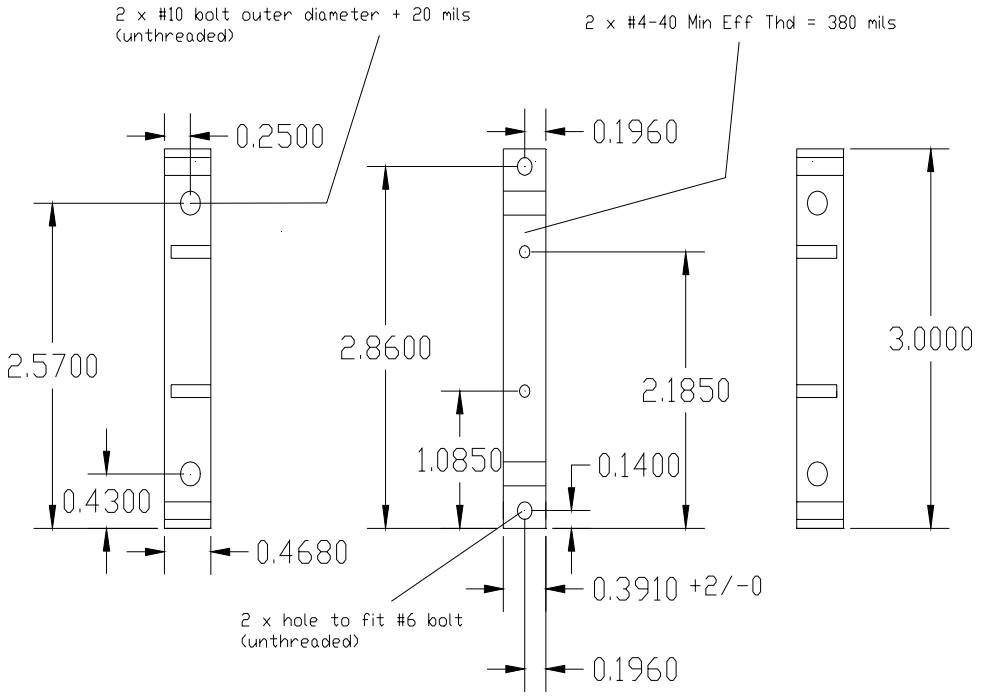


Figure 4. Copper Device Insert

7. Base plate drawing (Continued)

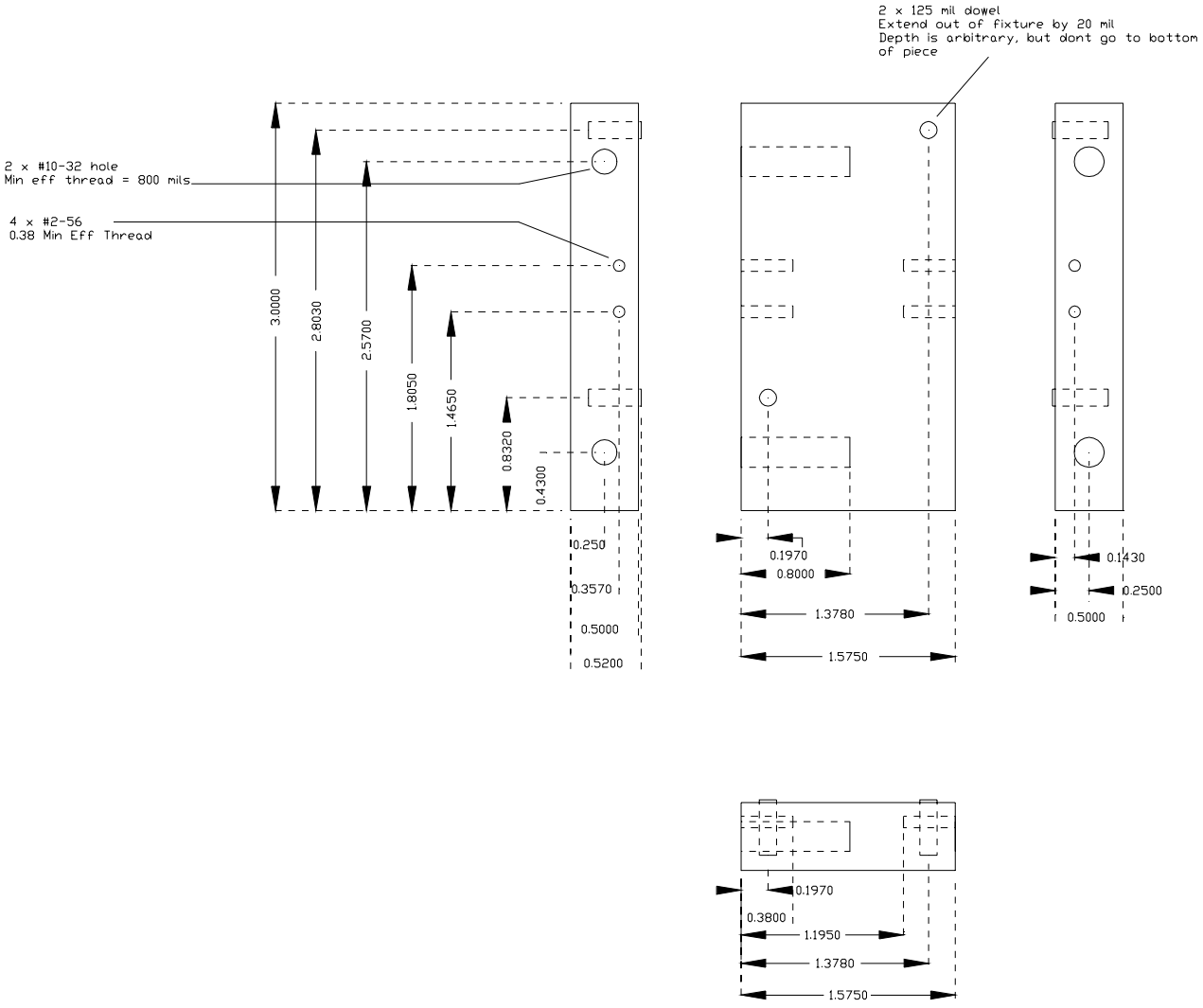


Figure 5. Brass Output Section